REPORT ON THREE DAY FACULTY DEVELOPMENT PROGRAM ON
"ANALOG IC DESIGN USING CADENCE TOOL"

The department of ECE has organized **three day** Faculty Development Program (FDP) on **"Analog IC Design Using CADENCE Tool"** during **12th December 2018 to 14th December 2018** at **VLSI lab** in ECE department from 9.30 A.M to 4.30 P.M.The department has invited the resource person **Mr.Sharath Kanth**, Senior Application Engineer**, Entuple Technologies Pvt. Ltd., Bangalore**.

The FDP aims to provide analog and digital IC design using Cadence tool. The Resource person explained about full and semi custom IC design flow and discussed which part of Cadence tool is used in each level of design. He explained analog full custom design and shown practical way of analysis step by step with simulation and layout design.

On second day of FDP, given clear analysis with physical verification using DRC and LVS checks and parasitic extraction using XRC tool. On third day, introduced ASIC design flow with example of design called "counter". He discussed with step by step design with RTL compiler, encounter and physical design with different steps like floor planning, routing, timing analysis and physical verification.

Faculty members of department actively participated in this FDP and this three day FDP was coordinated by Dr.K. Rajendra Prasad, Mr.T.Surender Reddy and Mr.V.Srinivas.

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